REMARKS

Amendments to the Claims

Claims 5 and 10-12 are amended. No new matter is added.

Claim 5 has been amended to further clarify that when the decoded next picture is a reference picture, it is stored into a frame buffer that is also not currently used to store a previous display picture. This is previously presented as step (b) in paragraph [0018]; no new matter has been added.

Claim 10 has been amended to include further details on the interlace/progressive converter, generating corresponding progressive video data "according to a previous display picture and a present display picture" (claim 10). Applicant points to paragraph [0051], which describes video data from a telecine source is displayed by the present invention by using "information of a present and a previous display picture". The same point is also inferred in paragraph [0050] for "performing motion adaptive de-interlacing operations incorporating video data of 3 through at most 8 fields stored" in memory. A minor typographical error is also corrected. No new matter is introduced.

Claims 11-12 has been amended in compliance with the amended claim 10.

Claim Objections – 35 USC §103

Claims 1-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuboi (US 6,912,254) in view of Suzuki (US 6,243,140).

Regarding claim 1, neither Tsuboi nor Suzuki teach or suggest that "if the decoded next picture is a B picture, buffering the decoded interlaced video data of the next picture into a frame buffer of the storage device not stored with a reference picture nor a present display picture nor a previous display picture". The Examiner asserts that Tsuboi discloses

the above-mentioned feature of claim 1 in Fig. 7 item 1, col. 11 line 41 to col. 12 line 27. However, as recited in Tsuboi in col. 11, lines 41~45, stating "When the piece of video data information to be stored in the frame memory is representative of the B-picture, the pieces of video data information are read out from the frame memories indicated by the variables "Core 0" and "Core 1".", Tsuboi does not disclose or teach "buffering the decoded interlaced video data of the next picture into a frame buffer of the storage device **not stored with a reference picture nor a present display picture nor a previous display picture**" (emphasis added). In particular, Tsuboi discloses "The frame memory controller 8A determines the frame memory A0/A1/A2/A3 to store a piece of video data information through a method shown in FIG. 10" in col. 9 lines 29-31, and "When the control signal 20 indicates that the bit string represents a B-picture, the answer at step S1 is given affirmative, and the frame memory controller 8A rewrites the variables "B", "Not Use" and an intermediate variable "temp"as by step S2. Namely, the frame memory controller 8A changes the variable "temp" to the reference code identical with that of the variable B, the variable B to the reference code identical with that of the variable "Not Use" and the variable "Not Use" to the reference code identical with that of the variable "temp". Thereafter, the frame memory controller 8A supplies the memory control signals 23/24/25 to the address generator 9, and causes the frame memory identified with the variable "B" to store the piece of video data information as by step S3. Thus, the reference code of the variable "B" is temporarily stored in the variable "temp", and the reference code of the intermediate variable "temp" is stored in the variable "Not Use". As a result, the piece of video data information is assigned to the unused frame memory, and is stored therein." in col. 9 lines 48-67.

Applicant respectfully points out utilizing the method shown in Fig. 10 of Tsuboi and the method of claim 1 as claimed in the present application to store video data in frame buffers would lead to different results. For example, if the decoded next picture is a B picture and the decoding sequence situation is RRRB, which is the example shown in Fig. 11 of Tsuboi, assuming that the fourth decoded picture is a B-picture B3 instead of reference

picture P3, Tsuboi teaches producing a frame memory sequence of "3", "1", "2", "0", "0", "1" (for frame memories indicated by the variables "Not Use", "Core 0", "Core 1", "B", "Write-In Frame Memory", and "Read-Out Frame Memory", respectively). In contrast, the present invention stores an incoming B-picture into a frame memory not already storing a reference picture, nor a previous or present display picture as claimed in claim 1. Thus, when applying the method of the present application to store video data in frame buffers in the above example, the resulting frame memory sequence would be "0", "1", "2", "3", "3", "1" (for frame memories indicated by the variables "Not Use", "Core 0", "Core 1", "B", "Write-In Frame Memory", and "Read-Out Frame Memory", respectively). Obviously, the B3 picture is stored in frame memory 3 since frame memories 0, 1, and 2 store references pictures while in Tsuboi, the B3 picture is stored in frame memory 0. Based on the different results between the Tsuboi and present invention, applicant believes it is clear that Tsuboi does not teach or disclose "if the decoded next picture is a B picture, buffering the decoded interlaced video data of the next picture into a frame buffer of the storage device not stored with a reference picture nor a present display picture nor a previous display picture" as recited in claim 1.

In view of the above, applicant respectfully submits that the Examiner has failed to show that any combination of Tsuboi and Suzuki would lead one of ordinary skill in the art to a method as claimed in claim 1, and in particular comprising "if the decoded next picture is a B picture, buffering the decoded interlaced video data of the next picture into a frame buffer of the storage device not stored with a reference picture nor a present display picture nor a previous display picture". Applicant respectfully submits that claim 1 is patentable over Tsuboi in view of Suzuki.

Claims 2-4 depend directly or indirectly on claim 1. Applicant submits that claims 2-4 should be found patentable over Tsuboi in view of Suzuki for at least the same reasons as presented for claim 1.

Regarding claim 5, neither Tsuboi nor Suzuki teach "if the decoded next picture is a

reference picture, buffering the decoded interlaced video data of the next picture into a frame buffer of the storage device not stored with the last decoded reference picture nor a present display picture **nor a previous display picture**" (emphasis added). The Examiner asserts that Tsuboi discloses the above-mentioned feature of claim 5 in Fig. 7 items 1, 2, col. 12 lines 3-27, 40-50.

However, Tsuboi discloses "On the other hand, if the control signal S20 indicates that the picture to be reproduced is a core picture, the answer at step S1 is given negative, and the frame memory controller 8A rewrites the variables "Core 0", "temp", "Core 1" and "Not Use" as by step S4. In detail, the frame memory controller 8A changes the intermediate variable "temp" to the reference code identical with that of the variable "Core 0", then the variable "Core 0" to the reference code identical with that of the variable "Core 1", then the variable "Core 1" to the reference identical with that of the variable "Not Use", and, finally, the variable "Not Use" to the reference code identical with that of the intermediate variable "temp". Thus, the variable "Core 1" is indicative of the frame memory to store the piece of video data information. The reference code of the variable "Core 1" is stored in the variable "Core 0", and the piece of video data information representative of a core picture one picture before the latest core picture is stored in the frame memory specified by the variable "Core 0". The previous reference code of the variable "Core 0" is useless, and is transferred to the variable "Not Use"" in col. 10 lines 1-21.

Particularly, according to the cited paragraphs and Fig. 11 of Tsuboi, when reference picture P3 is received after three reference pictures, previous reference pictures I0, P1, and P2 are stored in frame memories 0, 1, and 2, respectively. Tsuboi teaches the picture P3 will be stored in frame memory 0, where I0 was previously stored, by shifting variables pointing to the frame memories: "Core 0" moves to "Not Use", "Core 1" to "Core 0", and "Not Use" to "Core 1", while "B" remains unchanged. Thus, Tsuboi teaches P3 would be stored in frame memory 0, as shown in Fig. 11. In contrast, according to the method of claim 5 of the present invention stating "if the decoded next

picture is a reference picture, buffering the decoded interlaced video data of the next picture into a frame buffer of the storage device not stored with the last decoded reference picture nor a present display picture nor a previous display picture", the reference picture P3 would be stored in frame memory 3; that is, the variable "Write-In Frame Memory" would point to frame memory 3 since frame memories 0, 1, and 2 store a previous display picture, a present display picture, and a last decoded reference picture respectively. In view of the above, applicant respectfully submits that the Examiner has failed to show that any combination of Tsuboi and Suzuki would lead one of ordinary skill in the art to a method as claimed in claim 5, and in particular comprising "if the decoded next picture is a reference picture, buffering the decoded interlaced video data of the next picture into a frame buffer of the storage device not stored with the last decoded reference picture nor a present display picture nor a previous display picture". Applicant respectfully submits that claim 5 is patentable over Tsuboi in view of Suzuki.

Claims 6-9 are dependent upon their base claim 5 and are thus believed to be patentable over Tsuboi in view of Suzuki for at least the same reasons as those presented for claim 5.

Regarding claim 10, neither Tsuboi nor Suzuki teach "an interlace/progressive converter coupled to the storage device, for de-interlacing data stored in the frame buffers to generate corresponding progressive video data according to a previous display picture and a present display picture" (claim 10 excerpt). Applicant notes that even combining the teachings of Tsuboi and Suzuki would not produce the expected results of the present invention.

For instance, using Tsuboi's illustration in Fig. 11 as an example, if the fourth decoded picture was a B-picture (instead of the depicted P-picture P3 in Tsuboi), the frame buffering method taught by Tsuboi would produce a frame memory sequence of "3", "1", "2", "0", "0", "1" (for frame memories indicated by the variables "Not Use", "Core 0", "Core 1", "B", "Write-In Frame Memory", and "Read-Out Frame Memory", respectively). The

previous display picture which was stored in the frame memory 0 indicated by the variable "Read-Out Frame Memory" when the next picture was picture P2 will be overwritten by the picture B3 when the decoded data of the next picture is picture B3, because Tsuboi teaches changing the variable "Write-In Frame Memory" to "0" when the next picture is picture B3. Thus, since the previous display picture has been overwritten in its frame memory buffer, combining Tsuboi and Suzuki will not allow generating progressive video data (de-interlacing) "**according to the previous display picture and the present display picture**" (emphasis added).

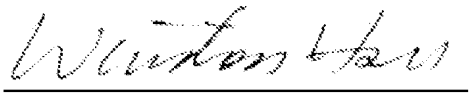
Similarly, as illustrated above, when the next picture is reference picture P3 as shown in Fig. 11 of Tsuboi, the resulting frame memory sequence is "1", "2", "0", "3", "0", "1" (for "Not Use", "Core 0", "Core 1", "B", "Write-In Frame Memory", and "Read-Out Frame Memory", respectively). Since the variable "Write-In Frame Memory" is changed to "0", the previous display picture which was stored in frame memory 0 is overwritten. Applicant respectfully points out that combining Tsuboi and Suzuki does not achieve the same results as presented in the interlace/progressive converter of claim 10, and as such, claim 10 is patentable over Tsuboi in view of Suzuki.

Claims 11-15 are dependent upon their base claim 10 and are thus believed to be patentable over Tsuboi in view of Suzuki for at least the same reasons as those presented for claim 10.

Conclusion

In view of the above, applicant submits that the application is now in condition for allowance and respectfully urges the Examiner to pass this case to issue. The Examiner is encouraged to telephone the undersigned if there are informalities that can be resolved in a phone conversation, or if the Examiner has any ideas or suggestions for further advancing the prosecution of this case.

Sincerely yours,



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